UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/428,052	10/27/1999	KIYOSHI IRINO	970901A	4139

38834 7590 05/05/2005

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/428,052	IRINO, KIYOSHI
	Examiner	Art Unit
	José R. Díaz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,10 and 15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,10 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/917,936.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 9, 2005 has been entered.

Claim Objections

2. Claim 16 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Please note that claim 6 recites the limitations recited in claim 16.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US Pat. No. 5,650,344) in view of applicant's admitted prior art, and further in view of Susuki (JP 09-064362 A).

Regarding claim 6, Ito et al. teaches a method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film (12) on a substrate (10) by a thermal oxide film (grown in a dry oxygen ambient) [col. 3, lines 25-26 and fig. 1B];

forming a gate electrode pattern (20) on said gate oxide film [fig. 1D];

forming diffusion regions (28, 30) in said substrate at both lateral sides of said gate electrode pattern (see fig. 1E) by introducing an impurity element (N-type or P-type) into said substrate through said gate oxide film while using said gate electrode pattern as a mask [col. 4, lines 33-35 and fig. 1E]; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask (nitriding the oxide film) [col. 3, lines 36-45 and fig. 1D], such that

said N atoms do not penetrate into the substrate (consider the nitriding step[1] of the SONO process) [col. 3, lines 36-41], and

said step of introducing said impurity said impurity element being conducted prior to said step of introducing N atoms into said gate oxide film [col. 4, lines 45-47 and col. 5, lines 55-59],

wherein said step of introducing N atoms into said gate oxide film (12) comprises a thermal annealing process of said gate oxide film [col. 4, lines45-47],

wherein activation of said impurity element is conducted simultaneously to said thermal annealing process [col. 4, lines 45-47].

However, Ito et al. fails to teach the limitation of forming a contact hole through said gate oxide film, and a thermal annealing process conducted in an atmosphere containing NO and at a temperature of about 800 °C.

Applicant's admitted prior art teaches that it is well known in the art to anneal the gate oxide film at a temperature of about 800 °C [page 5, lines 1-2 and figs. 3A-3B]. The motivation for doing so is to increase the nitrogen incorporation in the dielectric without a significant increase in oxide thickness.

Suzuki teaches that it is well known in the art to form a contact hole through said gate oxide film (see fig. 1D). The motivation for doing so is to provide an electrical connection to the source/drain region.

Ito et al., applicant's admitted prior art and Suzuki are analogous because they are from the same field of endeavor as applicant's invention. At the time of the invention

[1] See paragraph 8 under "Response to Arguments" on page 9 of this Office Action.

it would have been obvious to a person of ordinary skill in the art to include a nitridation process conducted in an atmosphere containing NO and at a temperature of about 800 °C, and to form a contact hole through said gate oxide film. The motivation for doing so is to increase the nitrogen incorporation in the dielectric without a significant increase in oxide thickness and to provide an electrical connection to the source/drain region. Therefore, it would have been obvious to combine Applicant's admitted prior art with Ito et al. to obtain the invention of claim 6.

6. Claim 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US Pat. No. 5,650,344) in view of applicant's admitted prior art and Susuki (JP 09-064362 A), and further in view of Kim et al. (US Pat. No. 5,464,783).

Regarding claims 15-16, Ito teaches the step of forming an oxide film (32) on said gate oxide film (12) [col. 4, lines 47-49) subsequently after said step of introducing N atoms (SONO process) [col. 4, lines 45-47].

However, the prior art fails to teach the limitation of forming a CVD oxide film continuously without taking out said semiconductor substrate out of a processing chamber.

Kim et al. further teaches that it is well known in the art to conduct a nitridation process and an oxide deposition process in the same CVD processing chamber (see col. 4, lines 12-16 and col. 3, lines 57-64).

Ito et al., applicant's admitted prior art, Susuki and Kim et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time

of the invention it would have been obvious to a person of ordinary skill in the art to conduct the nitridation process and the CVD oxide deposition in the same CVD processing chamber. The motivation for doing so, as is taught by Kim et al. (col. 4, lines 17-18), is minimizing handling of the substrate. Therefore, it would have been obvious to further combine Kim et al. with Ito et al., applicant's admitted prior art and Susuki to obtain the invention of claims 15-16.

Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loh et al. (US Pat. No. 5,516,707) in view of Susuki (JP 09-064362 A).

Regarding claim 10, Loh et al. teaches a method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film (35) on a substrate(20) [see fig. 1] by a thermal oxide film (grown) [see col. 2, lines 46-47];

forming a gate electrode pattern (26) on said gate oxide film such that said gate electrode pattern is in direct contact with said oxide film [see fig. 1];

forming diffusion regions (21, 22) in said substrate at both lateral sides of said gate electrode pattern [see fig. 1] by introducing an impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask [see col. 3, lines 4-12]; and

introducing N atoms (50), after said step of introducing said impurity element, into said gate oxide (35) film while using said gate electrode pattern (26) as a mask [see fig.

2], such that said N atoms do not penetrate into the substrate [please note that nitrogen are incorporated immediately above source/drain regions. See col. 3, lines 13-15], and

wherein said step of introducing N atoms into said gate oxide film includes an ion implantation process of N ions [col. 3, lines 15-16].

In addition, Loh et al. that it is well known in the art to optimize the implant process by controlling the implant dose, energy and tilted angle [see col. 3, lines 22-24].

However, Loh et al. fails to teach an acceleration voltage not exceeding 10 keV and a dose of 1-3 x 10^{14} cm^{-2}.

Suzuki teaches that it is well known in the art to implant ions in the gate oxide layer (2) at an acceleration voltage of between about 5-20 keV and a dose of 1-5 x 10^{14} cm^{-2} [see paragraph 0022 and fig. 1C].

Loh et al. and Suzuki are analogous because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to art to implant ions in the gate oxide layer at an acceleration voltage not exceeding 10 keV and a dose of 1-3 x 10^{14} cm^{-2}. The motivation for doing so, as is taught by Suzuki (abstract), is to improve the threshold voltage V_{TH} and dielectric strength of the gate oxide by increasing the nitrogen concentration in portions of gate oxide located above source/drain regions. Therefore, it would have been obvious to combine Applicant's admitted prior art with Ito et al. to obtain the invention of claims 10 and 18.

Regarding claim 18, Suzuki further teaches that said N atoms are incorporated into said gate oxide film with a concentration of about 3% [paragraph 0022].

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loh et al. (US Pat. No. 5,516,707) in view of Susuki (JP 09-064362 A), and further in view of Duane (US Pat .No. 5,804,496).

Regarding claim 17, Loh et al. teaches a tilted angled implant technique for incorporating nitrogen atoms (50) in the gate oxide [see fig. 2]. In addition, Loh et al. further teaches that it is well known to optimize the implant technique by controlling the implant dose, energy and tilted angle [col. 3, lines 22-25].

However, the prior art fails to teach implanting the nitrogen atoms at a perpendicular angle.

Duane teaches that it well kwon in the art to implant nitrogen atoms at 90° (col. 3, lines 65-67).

Loh et al., Suzuki and Duane are analogous because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to art to implant nitrogen ions at a perpendicular angle. The motivation for doing so, as is taught by Duane (col. 4, lines 65-67), is to introduce nitrogen ions without substantial penetration into active regions. Therefore, it would have been obvious to combine Duane with Loh et al. and Suzuki to obtain the invention of claim 17.

Response to Arguments

7. Applicant's arguments with respect to claims 6, 10, and 15-18 have been considered but are moot in view of the new ground(s) of rejection.

8. With regards to arguments that Ito et al fails teach the limitation of introducing the nitrogen atoms without penetrating the substrate, it is noted that the SONO process in Ito et al. includes two steps: a nitriding step [col. 3, lines 36-45] which incorporates nitrogen atoms over the width of the gate oxide, without reaching the substrate [col. 3, lines 43-45]; and a re-oxidizing step [col. 3, lines 46-49 and col. 4, lines 17-19], which further extends the nitrogen atoms into the region 24 of the substrate [col. 4, lines 17-19]. In addition, it is noted that claim 6 uses the term "comprising" which is inclusive or open-ended and does not exclude additional, unrecited elements or method steps (MPEP 2111.03). Thus, the fact that the nitrogen atoms are incorporated in the substrate during the subsequent re-oxidation step is irrelevant since claim 6 does not preclude performing this additional step in the claimed method. Therefore, the SONO process of Ito et al. makes obvious the claimed limitation by teaching a nitriding step that incorporates N atoms in the gate oxide such that the N atoms do not penetrate in the substrate.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

José R. Díaz
Examiner
Art Unit 2815